LISTING OF THE CLAIMS

1. (Previously presented) A method for testing a memory device comprising:

placing said memory device in a test mode;

resetting all match lines of said memory device;

confirming proper operation of a control line used to enable output from a match line under test;

enabling output from the match line under test;

decoding an address of a selected memory storage location corresponding to said match line under test;

loading said selected memory storage location and a comparand register with a known data pattern;

performing a search operation, for the known data pattern in the comparand register, on said memory device;

outputting a result of said search operation;

comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test;

confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and

indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation.

2. (Original) The method according to claim 1, wherein said memory device is a content addressable memory (CAM) device.

3. (Original) The method according to claim 1, further comprising:

resetting output from said match line under test; and

enabling output from said memory storage location under test.

4. (Original) The method according to claim 1, wherein said resetting and said decoding acts occur on the rising edge of a clock signal.

5. (Original) The method according to claim 1, wherein said loading acts occur on the rising edge of a clock signal.

6. (Original) The method according to claim 1, wherein there is a one-to-one correspondence between said match lines and said memory storage locations.

7. (Original) The method according to claim 1, wherein there is a one-to-many correspondence between each said match line and said memory storage locations.

8. (Previously presented) A method of testing a memory device that includes two or more sets of memory cells and, for each set of memory cells, a match line that provides a match signal when items of data stored in said set of memory cells match a data item stored in a comparand register, the method comprising:

confirming proper operation of a control line used to enable output from said match line of a set of memory cells being tested;

enabling said match line of the set of memory cells being tested and disabling match lines of other sets of memory cells;

storing items of data matching the data item stored in the comparand register in the set of memory cells being tested; and

receiving an output signal from said match line and determining whether said output signal indicates that said set of memory cells being tested has items of stored data that match the data item stored in a comparand register.

9. (Original) The method according to claim 8, in which said memory device is a content addressable memory (CAM) device.

10. (Previously presented) The method according to claim 8, in which each set of memory cells comprises a memory storage location associated with an address and the act of determining includes determining whether said output signals indicate addresses of said set of memory cells being tested.

11. (Canceled)

12. (Previously presented) An apparatus for testing a match line of a memory device, said apparatus comprising:

a memory storage location corresponding to a match line under test, said match line under test further having a corresponding word line;

a comparator coupled to at least one search line per CAM memory cell of said memory storage location; and

a circuit coupled to said match line under test, said corresponding word line, and a test mode match line reset signal, said circuit determining a status of the match line under test based on a result of a search operation and a signal on the match line under test after confirming proper operation of a control line used to generate a signal on the word line.

13. (Original) The apparatus according to claim 12, further comprising a priority encoder coupled to said circuit, said priority encoder outputting an address of said memory storage location corresponding to said match line under test if said match line under test is functioning properly.

14. (Original) The apparatus according to claim 12, wherein said memory device is a content addressable memory (CAM) device.

15-16. (Canceled)

17. (Previously presented) A memory circuit comprising:

a set of memory cells that store items of data;

comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register; and

enabling circuitry that enables a match line to provide said match signal as an output when said set of memory cells is being tested, said enabling circuitry enabling the match line after confirming proper operation of a control line.

18. (Canceled)

19. (Previously presented) The memory circuit according to claim 17, in which said set of memory cells stores said item of data, said memory circuit further comprising a word line that selects said set of memory cells, said enabling circuitry enabling said match line in response to a signal on said word line.

20. (Previously presented) A memory device comprising:

two or more sets of memory cells, each set of memory cells storing an item of data;

for each set of memory cells, comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register;

for each set of memory cells, enabling circuitry that enables a match line to provide said match signal as an output when said set of memory cells is being tested;

for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry enabling said match line in response to a signal on said word line, said enabling circuitry enabling the match line after confirming proper operation of a control line used to generate the signal on the word line; and

control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are enabled.

21. (Original) The memory device according to claim 20, in which said memory device is a content addressable memory (CAM) device.

22. (Previously presented) The memory device according to claim 20, in which each set of memory cells comprises a memory storage location associated with an address; the control circuitry determining whether said output signals indicate an address of said set of memory cells being tested.

23. (Previously presented) A processing system comprising:

a processor;

a content addressable memory (CAM) device coupled to said processor via a bus, said CAM device comprising circuitry for testing a match line of said CAM device, said CAM device further comprising:

a memory storage location corresponding to a match line under test, said match line under test further having a corresponding word line;

a comparator coupled to at least one search line per CAM memory cell of said memory storage location; and

a circuit coupled to said match line under test, said corresponding word line, and a test mode match line reset signal, said circuit determining a status of a write enable signal used to generate a signal on the word line and determining a status of the match

line under test based on a result of a search operation and a signal on the match line under test.

24-29. (Canceled)

30. (Previously presented) An integrated circuit comprising:

a set of memory cells that store items of data;

comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register; and

enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested.

31. (Canceled)

32. (Previously presented) The integrated circuit according to claim 30, in which said set of memory cells stores said item of data, said memory circuit further comprising a word line that selects said set of memory cells, said enabling circuitry enabling said single match line in response to a signal on said word line.

33. (Previously presented) An integrated circuit comprising:

two or more sets of memory cells, each set of memory cells storing an item of data;

for each set of memory cells, comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register;

for each set of memory cells, enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested;

for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry enabling said single match line in response to a signal on said word line; and

control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are enabled.

34. (Original) The integrated circuit according to claim 33, in which said memory device is a content addressable memory (CAM) device.

35. (Previously presented) The integrated circuit according to claim 33, in which each set of memory cells comprises a memory storage location associated with an address and the control circuitry determines whether said output signals indicate an address of said set of memory cells being tested.

36. (Previously presented) A router comprising:

a memory circuit that comprises:

a set of memory cells that store items of data;

comparison circuitry that that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register; and

enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested.

37. (Canceled)

38. (Previously presented) The router according to claim 36, said memory circuit further comprising a word line that selects said set of memory cells, said enabling circuitry enabling said single match line in response to a signal on said word line.

39. (Previously presented) A router comprising:

a memory device that comprises:

two or more sets of memory cells, each set of memory cells storing an item of data;

for each set of memory cells, comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register;

for each set of memory cells, enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested;

for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry enabling said single match line in response to a signal on said word line; and

control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are enabled.

40. (Original) The router according to claim 36, in which said memory device is a content addressable memory (CAM) device.

41. (Previously presented) The router according to claim 36, in which each set of memory cells comprises a memory storage location associated with an address and the control circuitry determines whether said output signals indicate an address of said set of memory cells being tested.

42. (Previously presented) A system comprising:

a processor;

a content addressable memory (CAM) device coupled to said processor via a bus, said CAM device comprising an apparatus for testing a match line of said CAM device, said apparatus further comprising:

a memory storage location corresponding to a match line under test, said match line under test further having a corresponding word line;

a comparator coupled to at least one search line per CAM memory cell of said memory storage location; and

a circuit coupled to said match line under test corresponding to said word line, and a test mode match line reset signal, wherein said circuit performs the following functions:

placing said memory device in a test mode;

resetting all match lines of said memory device;

confirming proper operation of a control line used to enable output from said match line under test;

enabling said match line under test;

decoding an address of a selected memory storage location corresponding to said match line under test;

loading said selected memory storage location with a known data pattern;

loading a comparand register with said known data pattern;

performing a search operation, for the known data pattern in the comparand register, on said memory device; and

outputting a result of said search operation;

comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test;

confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and

indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation.